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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,704	02/20/2004	Kozo Sakamoto	H6808.0043/P043	4193

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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/781,704	SAKAMOTO ET AL.	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-16* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: POWER MOSFET WITH REDUCED GATE RESISTANCE.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Burstein et al.. As to claim 1, Burstein et al., Figures 2 and 3A, discloses a power semiconductor device comprising a semiconductor chip (42)(col. 5, line 65) in which a first main electrode (74), a second main electrode (76) and a control electrode (78)(col. 6, lines 34-46) are formed, wherein: a plurality of control electrode pads (78) are provided on said semiconductor chip, said plurality of control electrode pads being disposed within the periphery of a gate area, near the bottom edge of the chip (42), of said power semiconductor device, wherein said plurality of control electrode pads are connected to an electrode layer (44) disposed outside said semiconductor chip via a conductive bonding member (56).

As to claim 3, the scale of Burstein et al., Figure 3A, indicates that the horizontal distance between neighboring control pads is 295 μm. The figure also discloses that the distance between the left-most group of four control pads and the right-most group of four control pads is about 900 μm, making the total distance between the control pads which are furthest from each other about 295 μm + 900 μm + 295 μm, or about 1490 μm, which is within the scope of being 1500 μm.

As to claim 4, Burstein et al., Figure 3A, discloses that the semiconductor chip comprises a first main surface and a second main surface, wherein said control electrode pads (78) are disposed on said first main surface and said second main electrode (76) is formed on said second main surface.

Claims 5-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Burstein et al.. As to claim 5, Burstein et al., Figures 2 and 3A, discloses a power semiconductor device comprising a semiconductor chip (42) in which a first semiconductor area forming a first main electrode (74), a second semiconductor area forming a second main electrode (76) and a control electrode area forming a control electrode (78) are formed, wherein: a planar pattern is formed in said power semiconductor device, said planar pattern comprising a repetition of unit patterns made up of said first semiconductor area, said second semiconductor area and said control electrode area, wherein said first semiconductor area in the repeating planar pattern is connected to a plurality of first main electrode pads, said control electrode area are connected to a plurality of control electrode pads, and said second semiconductor area is connected to a plurality of second main electrode pads, wherein said first main electrode pads are connected via a plurality of conductive bonding members (56) to a metal electrode layer (44) disposed outside said semiconductor chip, and wherein said second main electrode pads are connected via another plurality of conductive bonding members (56) to another metal electrode layer.

As to claim 6, Burstein et al., Figure 2, discloses (col. 5, lines 53-57) that the metal electrode layers are separated from each other electrically, in order to carry the source and drain signals separately, but they are still formed on the same layer, one of (50) or (52).

As to claim 7, Burstein et al., Figures 2 and 3A, discloses that said control electrode area is connected via a first control-area conductive bonding member (56) to a control-area metal layer (50) disposed outside said semiconductor chip, and wherein the control-area metal layer (50) is extended over its active area and connected to a second control-area conductive bonding member (52) spaced from said first control-area conductive bonding member.

As to claim 8, Burstein et al. discloses (col. 1, line 51) that said semiconductor chip is a silicon semiconductor chip.

As to claim 9, Burstein et al. discloses that said semiconductor device is a power MOSFET in which said first main electrode is the source electrode (col. 6, line 35), said second main electrode is the drain electrode (col. 6, line 35), and said control electrode is the gate electrode of said power MOSFET (col. 6, lines 45-46).

Claims 10 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Burstein et al.. As to claim 10, Burstein et al., Figures 2, 3A, and 3C, discloses a power semiconductor device comprising a power semiconductor device formed in a semiconductor chip (42), said power semiconductor device comprising a first control electrode pad {one of (78)} for an external electrode, a second control electrode pad {one of (78)} disposed away from said first control electrode pad, and a gate control circuit for said power semiconductor device (col. 6, lines 45-46), said gate control circuit being disposed between said first control electrode pad and the source of said power transistor, and wherein said second control electrode pad is connected to the gate of said power transistor. Burstein et al., Figure 3C, discloses that the gate lines are all ganged together to form a common interconnection, which is within the scope of having said first control electrode pad is connected to said second control electrode pad via a conductive bonding member.

As to claim 11, Burstein et al. discloses that the power semiconductor device further comprises an external control-electrode pad, wherein a control circuit for said power transistor is provided between said external control-electrode pad and said first control electrode pad {one of (78)}, and wherein said first control electrode pad is connected to said second control electrode pad via a conductive bonding member.

Claims 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Burstein et al.. Burstein et al., Figure 2 and 3A, discloses a power semiconductor device comprising a plurality of control electrode pads (78) for the power semiconductor device formed within a semiconductor chip, wherein the control electrode pads are distributed within the periphery of the gate area (col. 6, lines 45-47).

As to claim 13, Burstein et al., Figures 2 and 3A, discloses that the control electrode pads (78) are connected via bumps (56) to an electrode layer disposed outside the semiconductor chip.

Claim 14-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Burstein et al.. As to claim 14, Burstein et al., Figure 2 and 3A, discloses a power semiconductor device, comprising a semiconductor chip (42) with a plurality of power transistors with a plurality of pads for control electrodes (78) of the semiconductor device, a first electrode layer (52) disposed outside said semiconductor chip, said first electrode layer is contacted to said pads with conductive bonding materials (56) and (54).

As to claim 15, Burstein et al., Figures 2 and 3A, discloses that the pads are formed apart from each other.

As to claim 16, Burstein et al., Figures 2 and 3A, discloses that said plurality of power transistors includes a plurality of pads for source and/or drain electrodes (74) and (76) of the semiconductor device, second electrode layers (50) different from said first electrode layer disposed outside said semiconductor chip, said second electrode layers is contacted to said pads for source and/or drain electrodes of said power semiconductor device with conductive bonding materials (56).

Allowable Subject Matter

Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention where the active area of the power device is formed between the furthest-most separated control electrode pads.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
March 16, 2005

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800